Influence of Different Recess Technology in GaN HEMTs

Sunil Kumar, Vimal Kumar Agrawal

Abstract— Recess Technologies in GaN HEMTs were simulated to check the influence of recess in device improvement process.In this work different recess are consider and their influence on the device characteristic is carried out. Gate recess improves device transconductance but main drawback of this is reduction in drain current. For most of the sensing and communication device applications both drain current (I_d) and transconductance (g_m) should be reasonably high. To achive this different recess depths combination are simulated a combination of 10nm Gate and Ohmic recess shows good balanced value of transconductance (g_m) and drain current(I_d) without any leakage current.

Index Terms— HEMT, GaN, Recess, Gate, Ohmic, Transconductance, Drain Current.

1 INTRODUCTION

High g_m and high I_d are essential in realizing the full potential of AlGaN/GaN HEMTs for sensing and communication applications as these parameters directly decide the sensitivity and response time. Gate recess is a well-known and a direct method of increasing the device g_m. However, its weak point is the reduction in I_d. It is thus obvious that gate recess all alone is not enough to fulfill the requirements for marked sensitivity and response time levels together. Next choice is combining the Gate recess with Ohmic recess [1]. As Ohmic recess has proved to reduce the contact resistance [2] and hence increased I_d. In this paper, we present a detailed simulation work on seperate and combined Ohmic and Gate recess. An analysis on various recess depths is given to achieve an optimized value and combination for good g_m and I_d without any leakage current.

2 SIMULATION AND RESUTS

High data-rate is desirable in many recent wireless multi-media. A non-recessed basic device case (A) of 1x100 µm used for simulation had an AlGaN layer of 25 nm and a GaN buffer of 2.7 µm. Table 1 summarizes all types of re-cess technology cases.Fig. 1(a,b,c), 2(a,b,c) and 3(a,b,c) shows the resulting I_d, g_m and I_g characteristics corresponding to the above Ohmic and Gate recess technology cases.

High g_m could result in high device sensitivity but low current at the same time could limit the device performance in terms of response time. Hence the degradation in the current stood as a pitfall in achieving required device performance as previously observed in Gate recess technology. In order to overcome this drawback we adopted a design technology where we etch the AlGaN layer and recess the ohmic contacts. The ohmic contacts recess are responsible for an increased value of the current and reduce contact resistance[1]. Hence we carried out simulations by recessing ohmic contacts.

TABLE 1
DIFFERENT DEVICETECHNOLOGY CASES

S.No	Device Technology	Cases
1.	Non-Recess	A
2.	Ohmic Recess	B above supply layer(10nm)
3.	Gate Recess	C(10nm)
4.	Ohmic+Gate Recess	D(10nm+10nm)

In order to study the effect o f change in the Ohmic recess device technology. Mainly, the effect on the current density and the transconductance were observed and compared as these both are the main factors influencing the device performance. It shows a drain current increase from 0.85 A/mm (non recessed case) to 0.90 A/mm for case B when barrier layer is etched as shown in Fig. 1(a). Same g_m 211 mS/mm as shown in Fig 1(b). But high gate leakage current flows in case of non recessed case A and ohmic recess case B. both as shown in Fig 1(c). Leakage current in all the Ohmic recess technology was believed to be a component of tunneling current between source and drain due to reduced contact resistance. So Ohmic recess technology could be a good choice for high power application but these devices are not acceptable for biosensing applications.

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High transconductance (g_m) and high drain – source current (I_{ds}) without leakage are essential in HEMTs for high power, high voltage and biosensing applications. So to increase g_m Gate recess technology is used [3].

In order to study the effect of change in the device technology, a systematic variation was made in the recessing gate contact up to a certain depth. It shows a drain current decrease from 0.85 A/mm (non recessed case) to 0.36 A/mm for case C as shown in Fig.2(a) . A corresponding change in the g_m shows which increased from 211 mS/mm (non recessed case) to 441 mS/mm for case C as shown in Fig 2(b). But high gate leakage current flows in case of non recessed case A as shown in Fig 2(c).

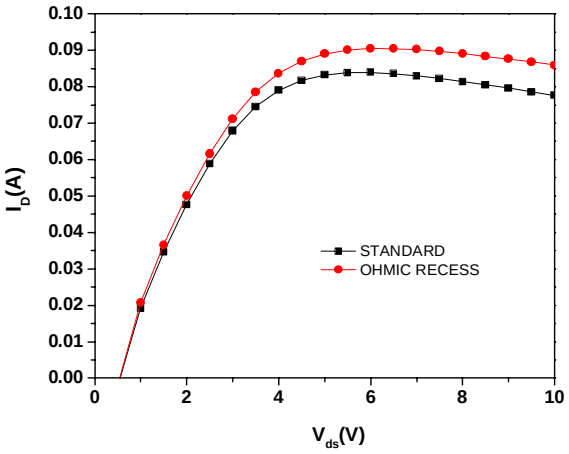

Fig1a. Drain current of non recessed and ohmic recess .

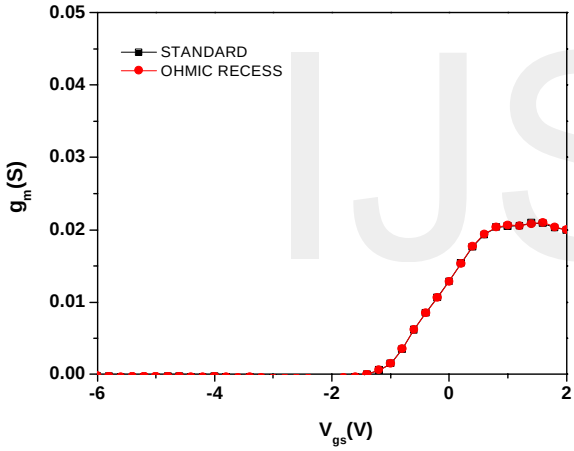

Fig1b. Transconductance of non recessed and ohmic recess.

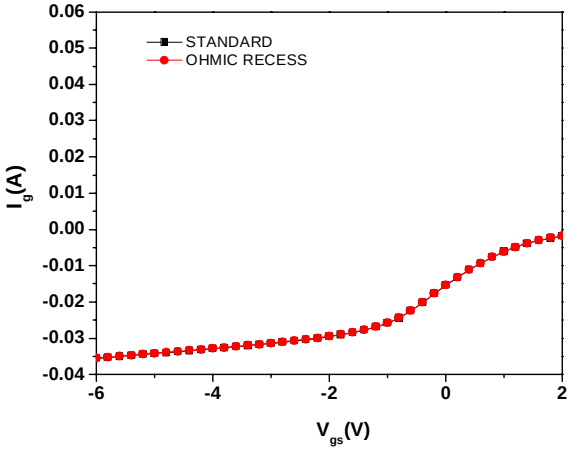

Fig1c. Leakage current of non recessed and ohmic recess .

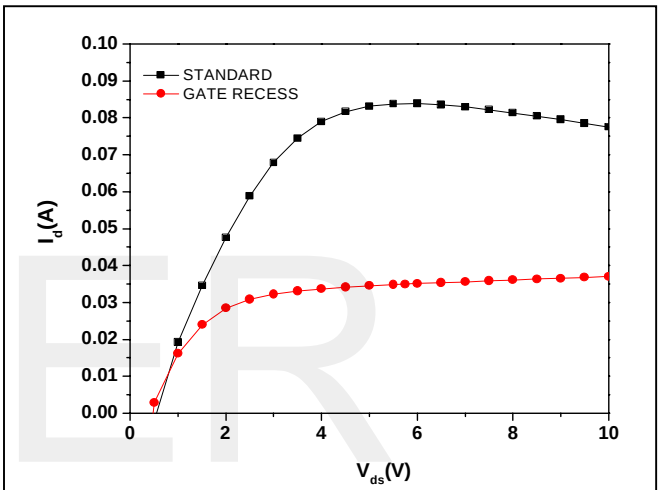

Fig2a. Drain current of non recessed and gate recess

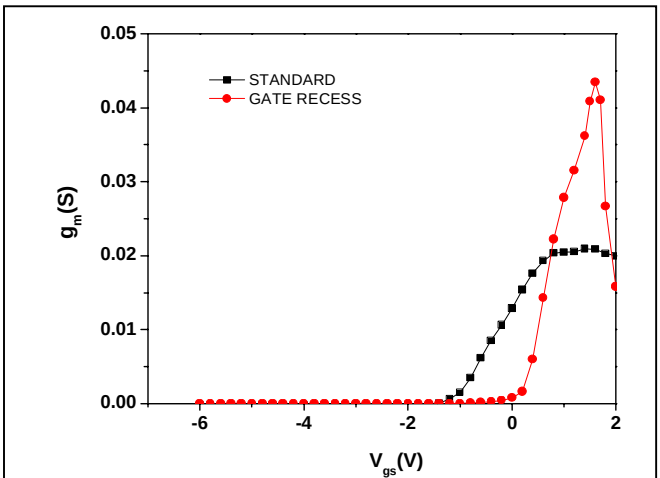

Fig2b. Transconductance of non recessed and gate recess .

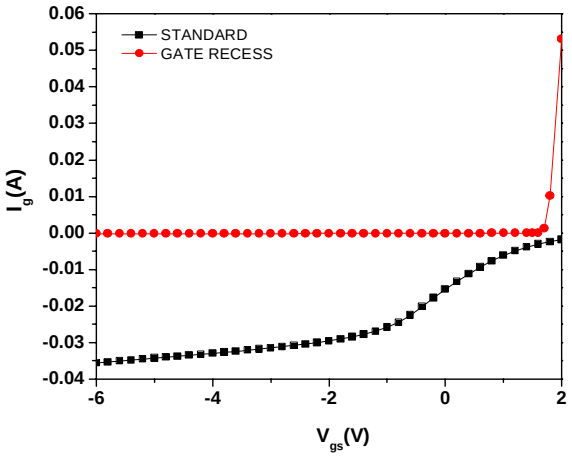

Fig2c. Leakage current of non recessed and gate recess .

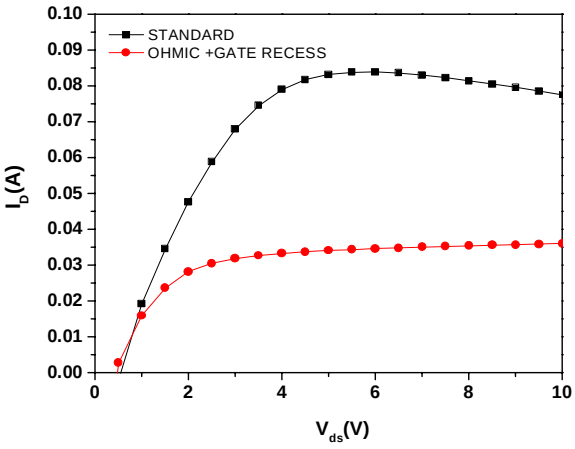

Fig3a. Drain current of non recessed and ohmic gate recess .

Since the case C showed the highest g_m due to highest recorded electric field, mobility μ and reduced gate channel distance. It seems to be a good choice for good response time and high sensitivity applications but it shows minimum I_d . Case A showed highest drain current but there is high amount of leakage current

As we studied and simulated Ohmic recess and Gate recess technologies in previous sections Ohmic recess improved drain current (I_d) but devices suffered with high gate leakage current and Gate recess improved device transconductance (g_m) but I_d reduced. High gate leakage current reduces the reliability and efficiency of the devices. But both the high transconductance (g_m) and high drain-source current (I_d) without leakage are essential in realizing the full potential of AlGaN/GaN HEMTs for high power, high voltage and biosensing applications and to improve noise performance and reliability. So switch on combined ohmic with Gate recess technology to achieve a balanced good I_d as well as g_m without any leakage.

Maximum increase in the transconductance was observed in fig 3b for case D whereas drain current I_d exceptionally decrease as in fig 3a in comparison to non recessed case A, Gate recess case B and Ohmic recess case C without any leakage current as shown in fig3c.

This was probably due to discontinued tunneling component path as a result of Gate recess in combination with Ohmic recess, I_d reduced due to a recorded reduction in the Electric Field [2]. However the g_m increased in both of the cases due to reduced gate to channel distance.

Interestingly, In Case D (10 nm, 10 nm) showed a good balance between g_m and I_d without any leakage. Hence, it was considered as an optimum and critical Ohmic and Gate recess depth combination.

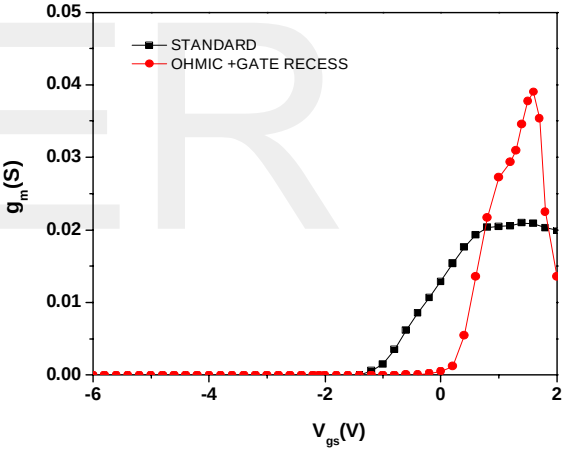

Fig3b. Transconductance of non recessed and ohmic gate recess .

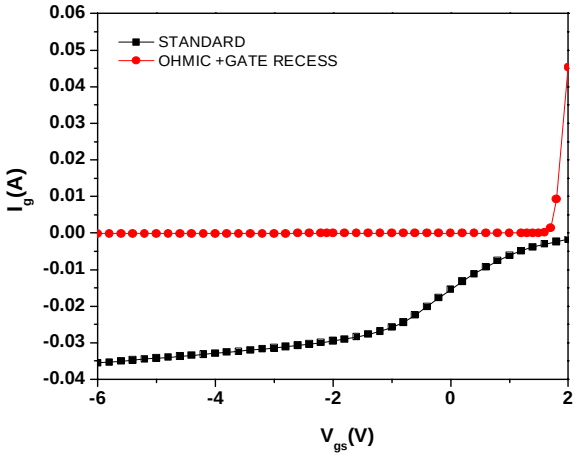

Fig3c. Leakage current of non recessed and ohmic gate recess.

3 Conclusion & Discussion

Simulations were performed to increase the g_m and I_d of GaN HEMTs and thereby simultaneously improving the sensitivity and response time of related sensors. In terms of device technology, a simulated Gate recess technology proved appropriate to increase the g_m. However it reduced the drain current which directly should affects the sensor's response. A combined Gate and Ohmic recess technology with a fixed and a critical value of Gate recess depth seemed to be the best approach to increase both g_m and I_d. Separate and combined Ohmic and Gate recess were simulated to attain good enough values of g_m and I_d without any leakage current I_g .Gate recess showed high g_m but reduced I_d. Ohmic recess showed high I_d but with high leakage current. Combined Ohmic and Gate recess technology cases did not show any leakage current. An optimized combined case D (10 nm+10 nm) showed good enough values of g_m and I_d without any leakage. Combined depths could be further optimized to increase the values of g_m and I_d for betterment in the device performance.

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